

FIG. 1

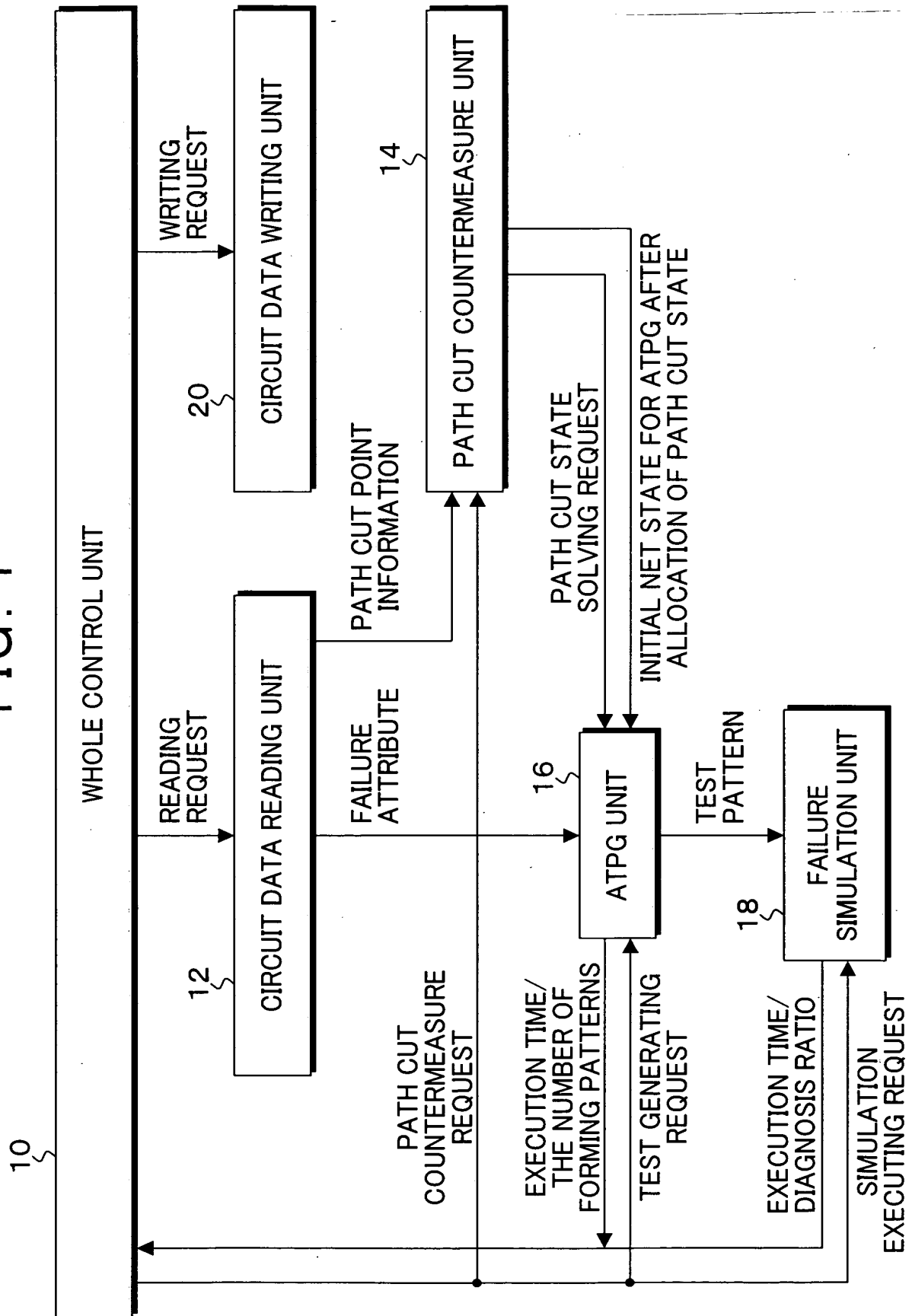


FIG. 2

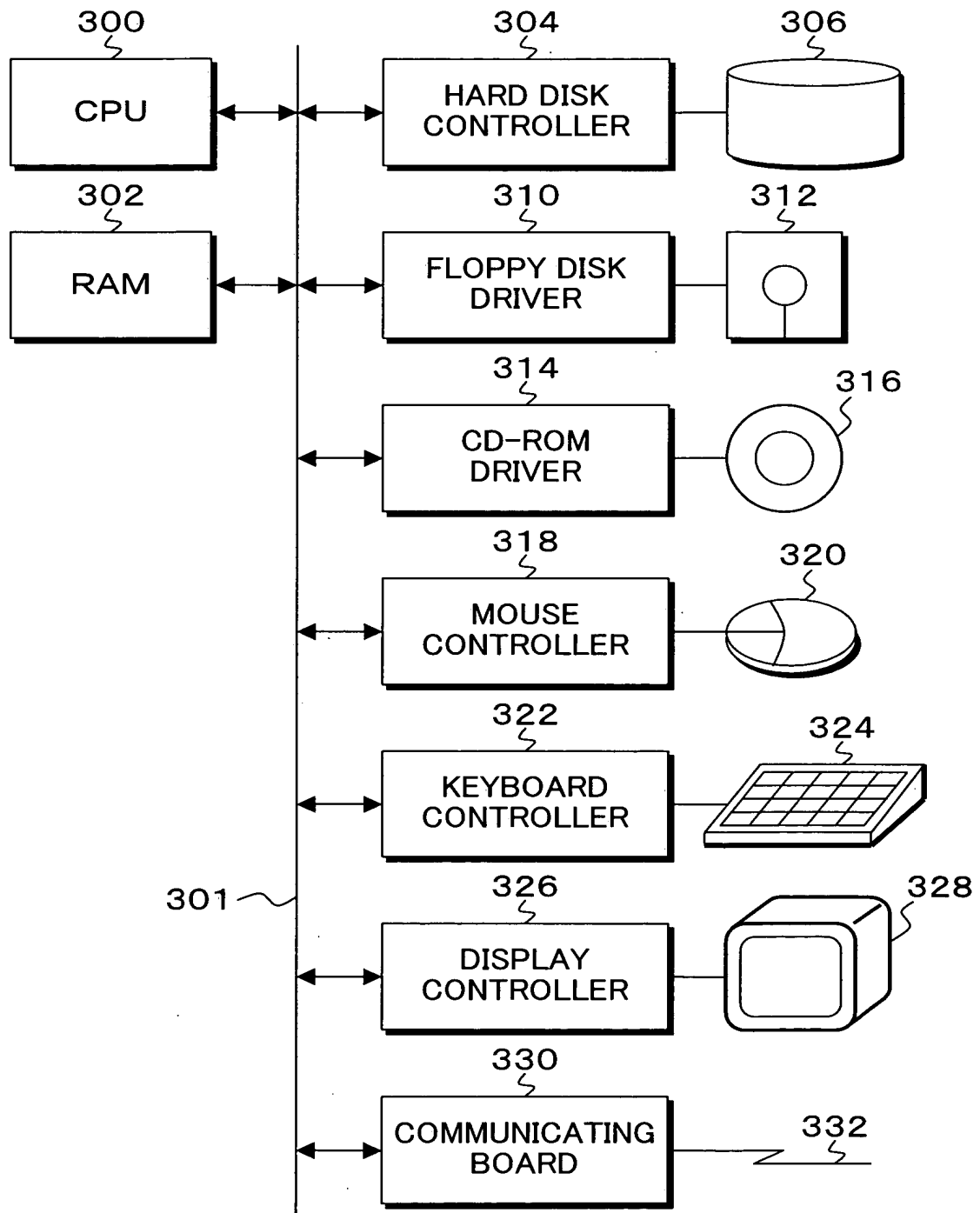


FIG. 3

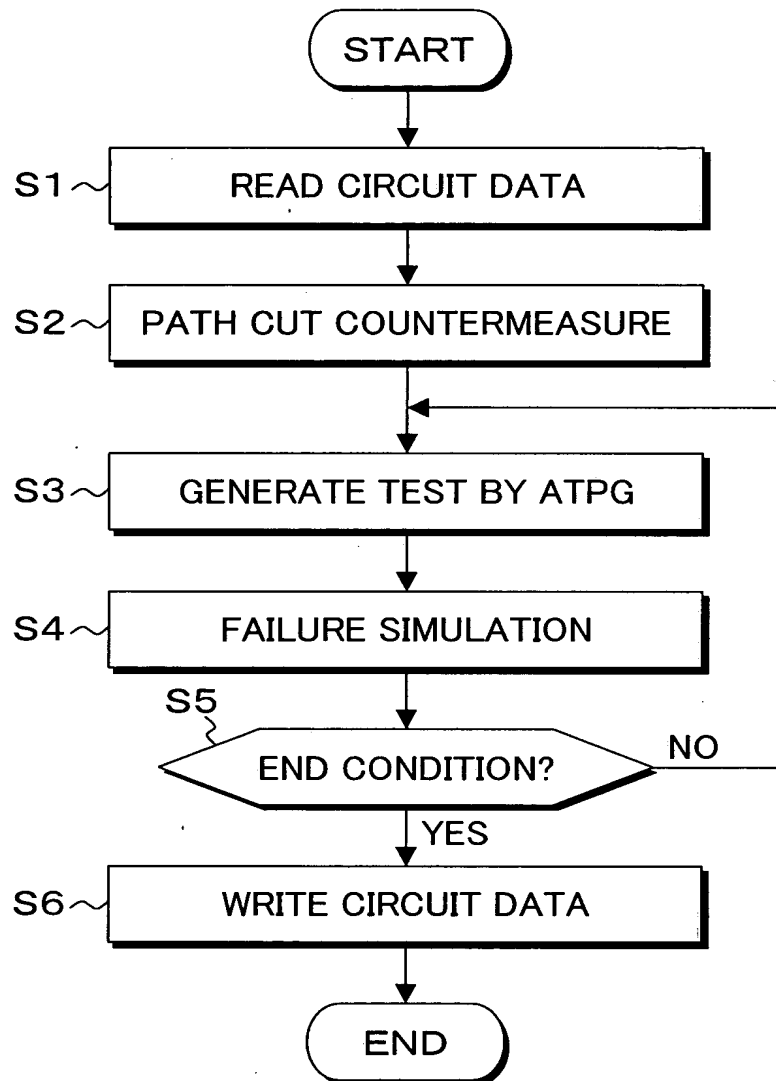


FIG. 4

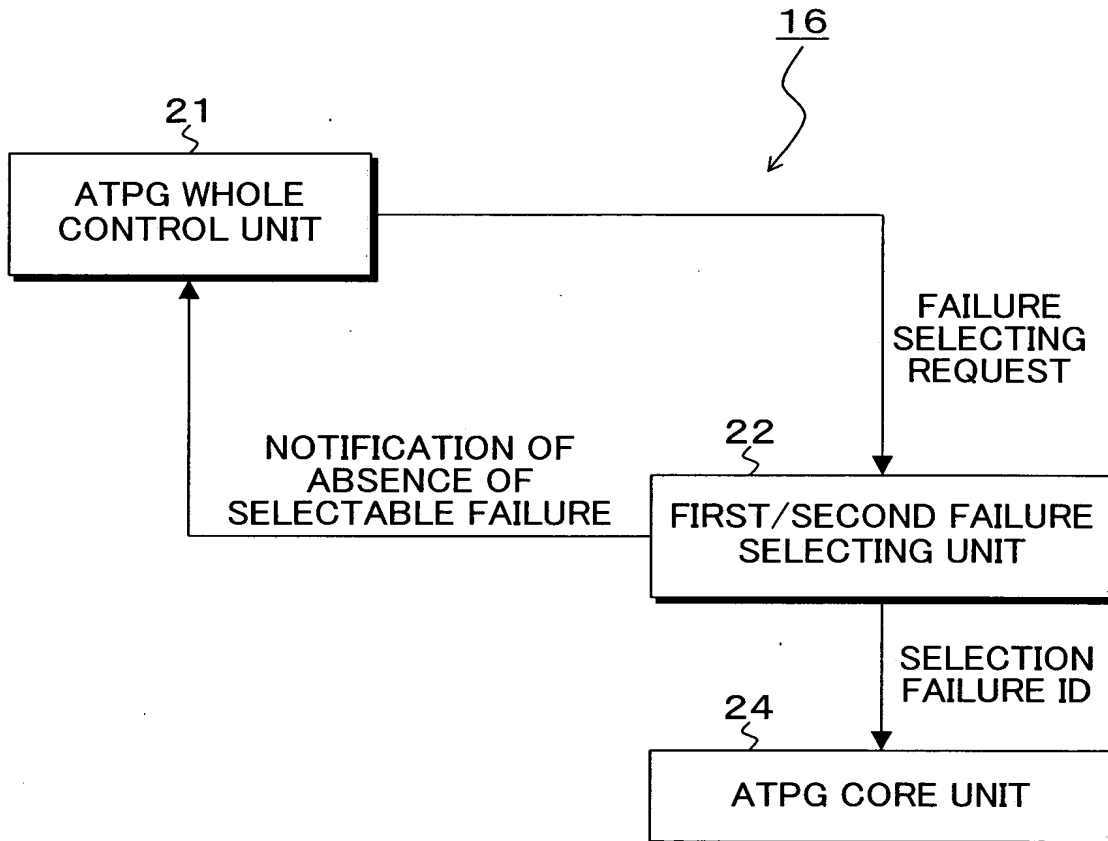


FIG. 5

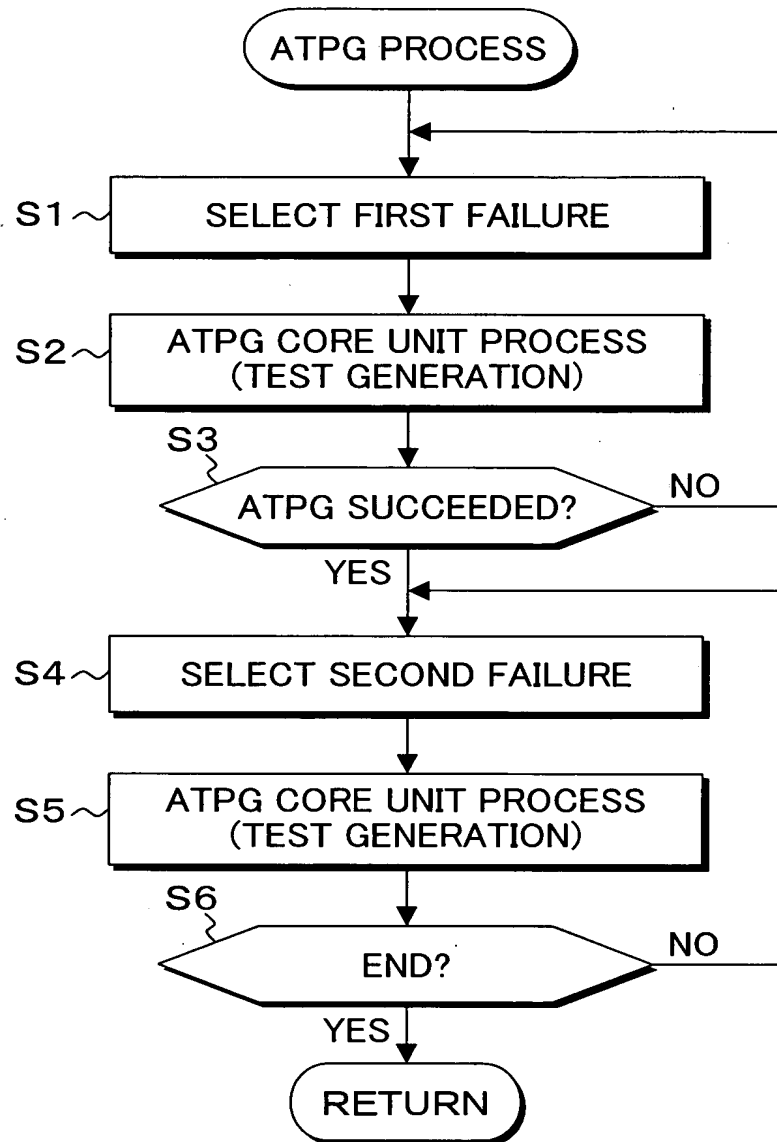
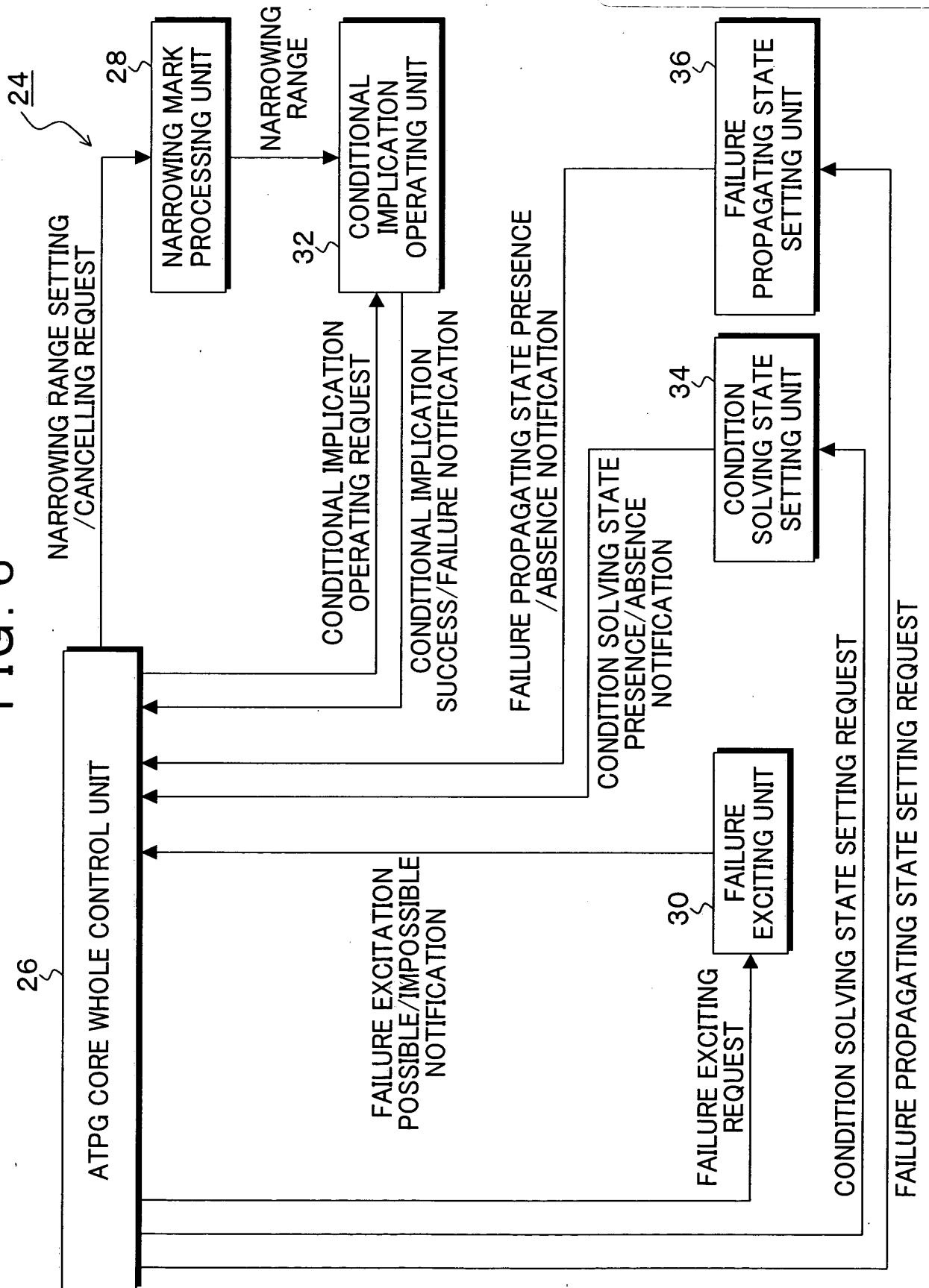


FIG. 6



7/35

FIG. 7A

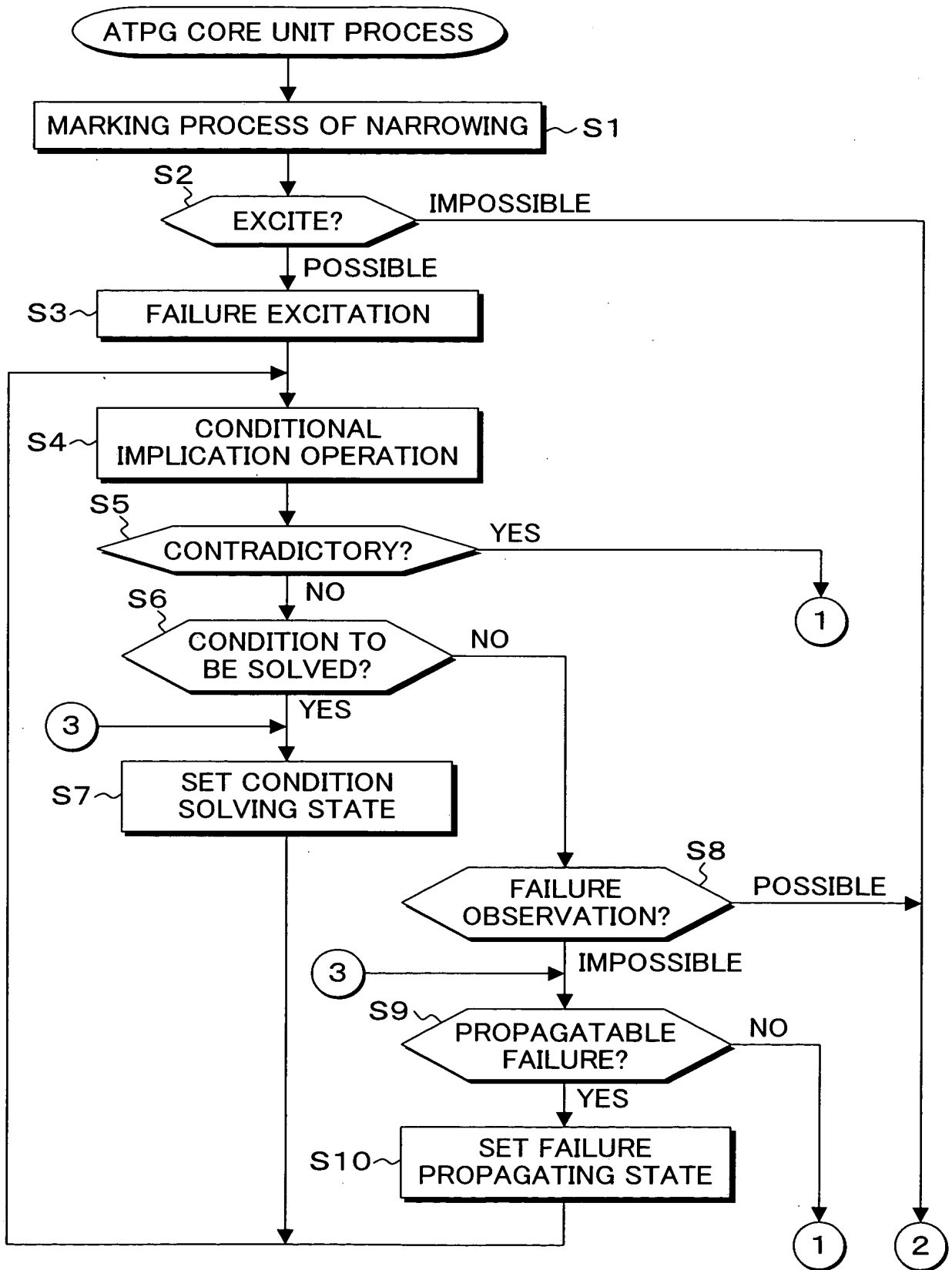


FIG. 7B

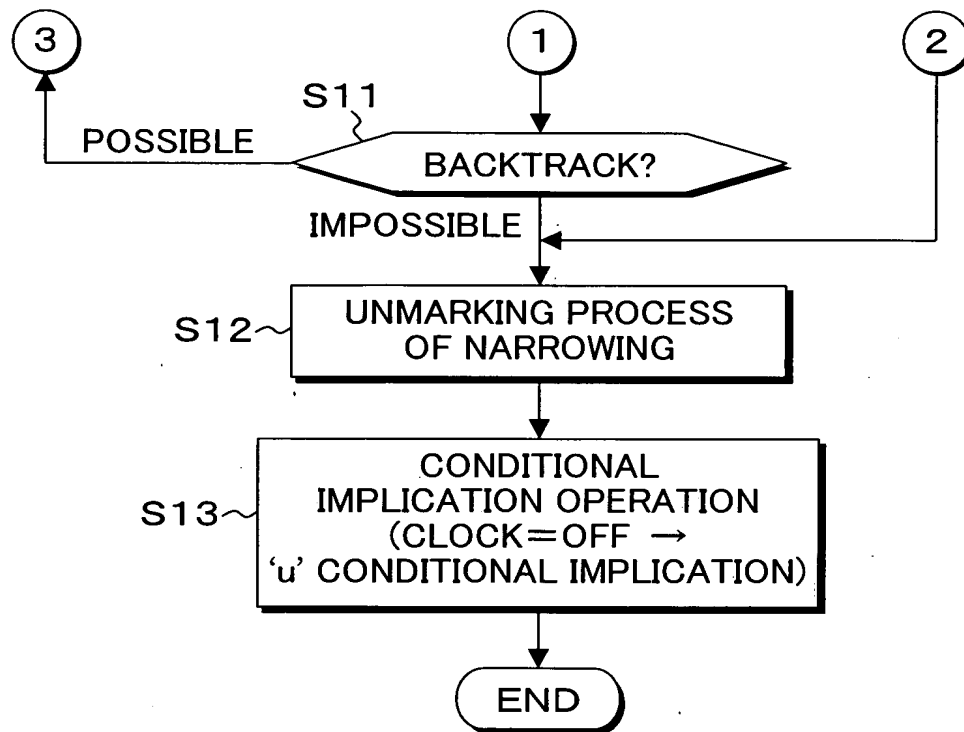


FIG. 8

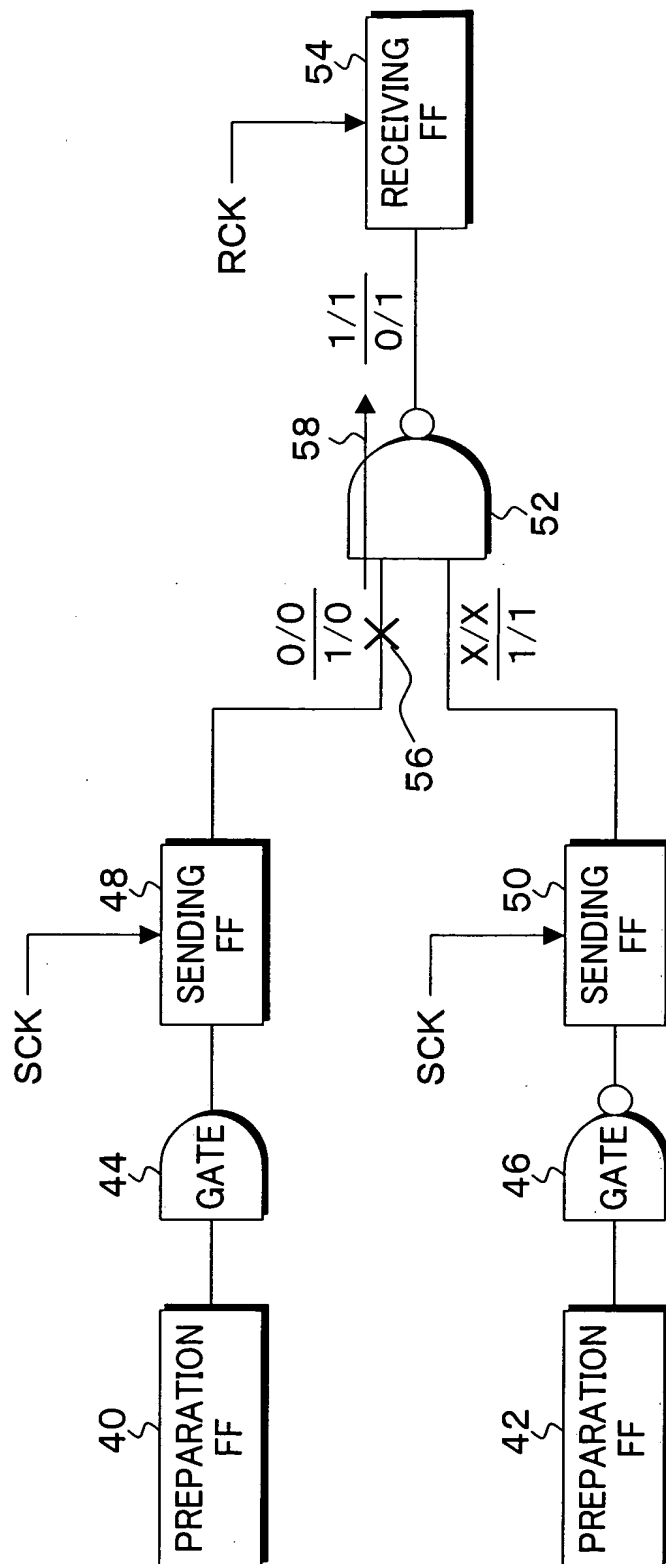


FIG. 9A
LEADING FAILURE
EXCITATION

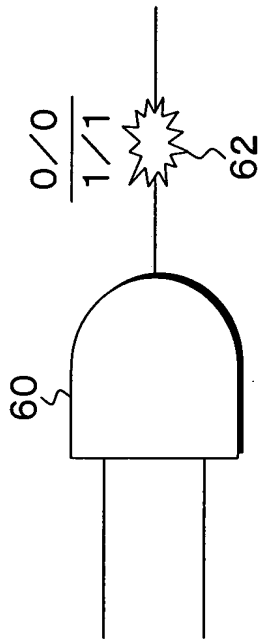


FIG. 9B
NORMAL

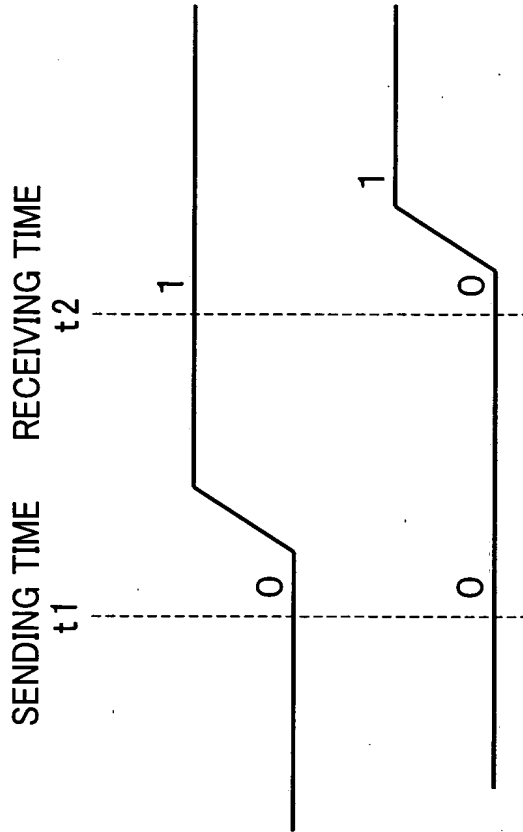


FIG. 9C
DELAY FAILURE

FIG. 9D
NOTATION

$$\frac{\text{SENDING TIME NORMAL VALUE/SENDING TIME FAILURE VALUE}}{\text{RECEIVING TIME NORMAL VALUE/RECEIVING TIME FAILURE VALUE}} = \frac{0/0}{1/0}$$

FIG. 10A
TRAILING FAILURE
EXCITATION

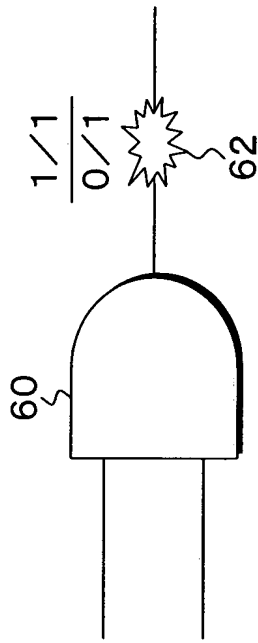


FIG. 10B
NORMAL

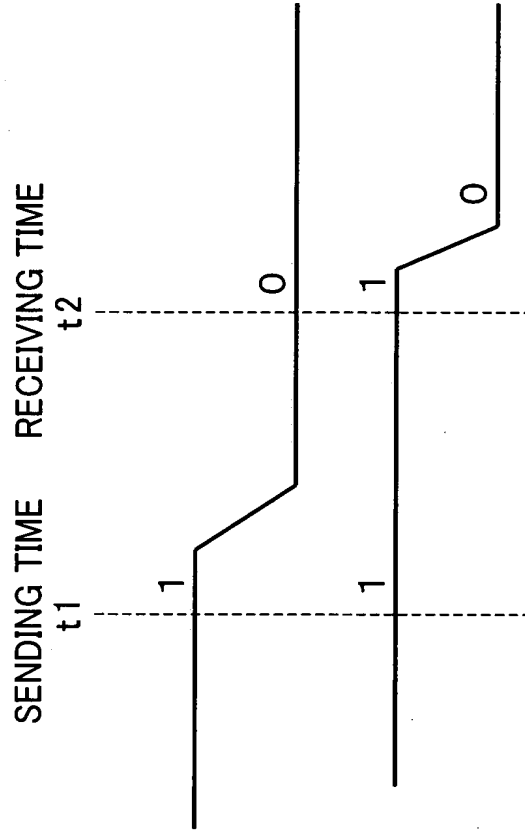


FIG. 10C
DELAY FAILURE

FIG. 10D
NOTATION

$$\frac{\text{SENDING TIME NORMAL VALUE/SENDING TIME FAILURE VALUE}}{\text{RECEIVING TIME NORMAL VALUE/RECEIVING TIME FAILURE VALUE}} = \frac{1/1}{0/1}$$

FIG. 11A

$$\frac{0/0}{0/0}$$

FIG. 11B

$$\frac{1/1}{1/1}$$

FIG. 11C

$$\frac{X/X}{0/0}$$

FIG. 11D

$$\frac{X/X}{1/1}$$

FIG. 11E

$$\frac{1/1}{0/0}$$

FIG. 11F

$$\frac{0/0}{1/1}$$

FIG. 12A

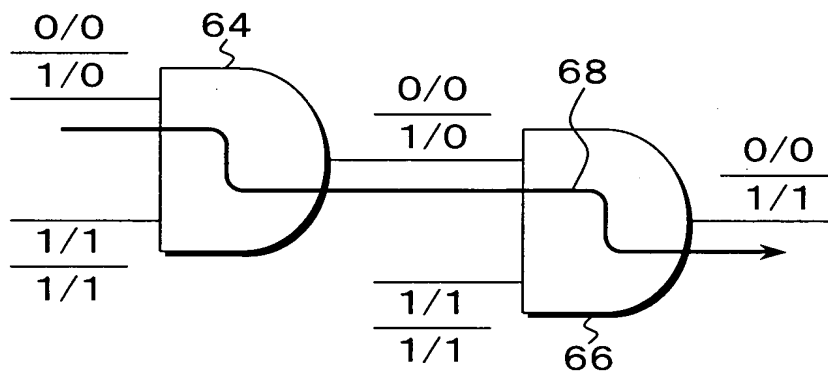
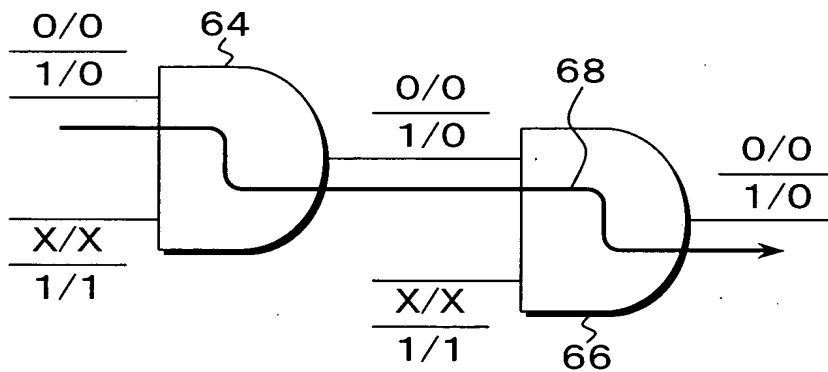


FIG. 12B



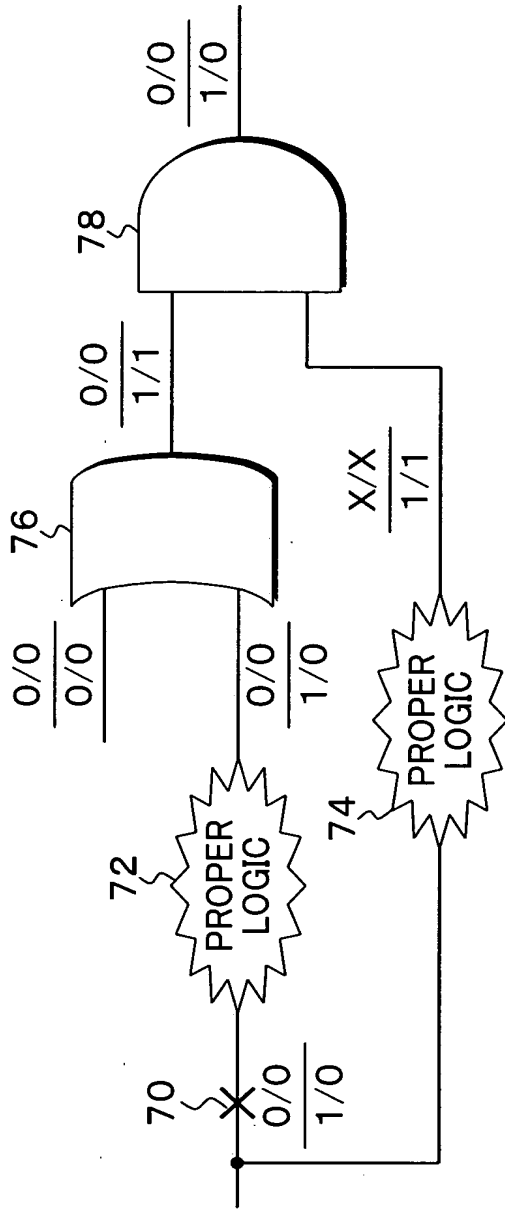


FIG. 13A

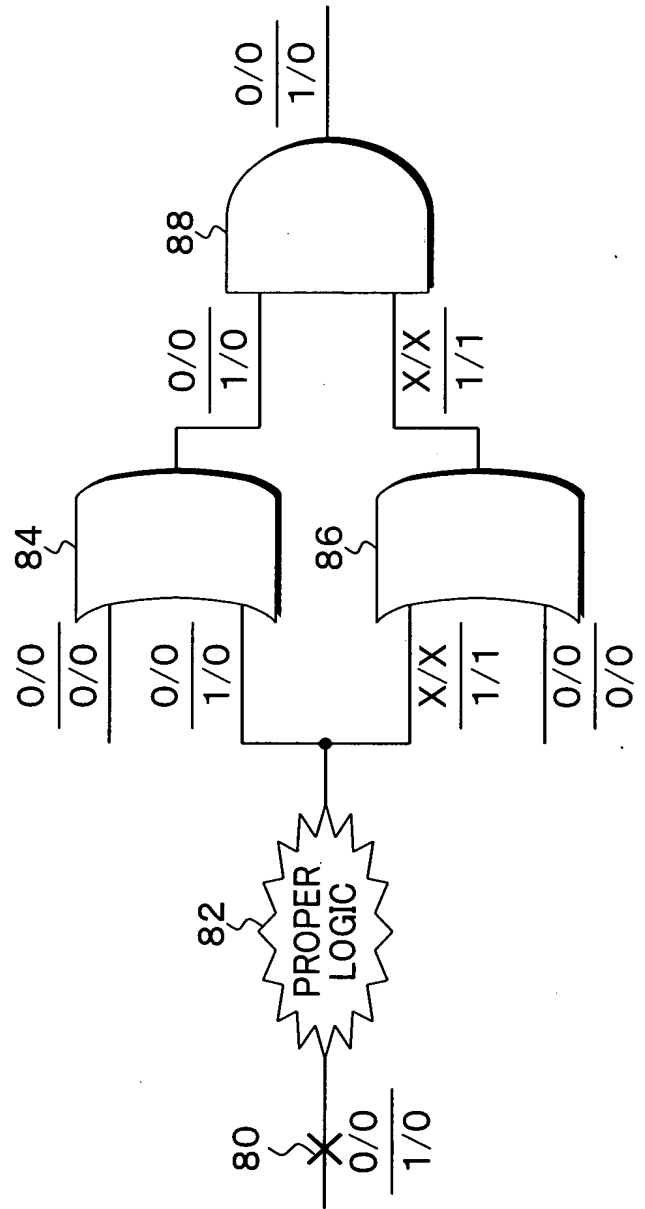


FIG. 13B

Figure 1 is a block diagram of a data transfer system. The system includes a D INPUT, three SENDING FF (First Flip) blocks (90, 92, 94), a RECEIVING FF block (100), and several logic gates (96, 98) and multiplexers (101, 103, 105, 107, 109). The diagram shows the flow of data from the D INPUT through the SENDING FF blocks and logic gates to the RECEIVING FF block. Various signals are labeled with numbers 90 through 109, and some signals are shown as outputs of the SENDING FF blocks (e.g., 1/1, X/X, 0/0, 1/1).

Figure 1 is a block diagram of a data transfer system. The system includes three 'SENDING FF' blocks (90, 92, 94) and one 'RECEIVING FF' block (100). Each 'SENDING FF' block has a 'SCK ON' input and a '0/0 1/1' output. The outputs of the 'SENDING FF' blocks are connected to a series of logic gates (96, 98, 102, 104, 106, 108, 110, 112) which perform bit-wise operations (AND, OR, XOR) on the data. The final output is connected to the 'RECEIVING FF' block.

FIG. 15

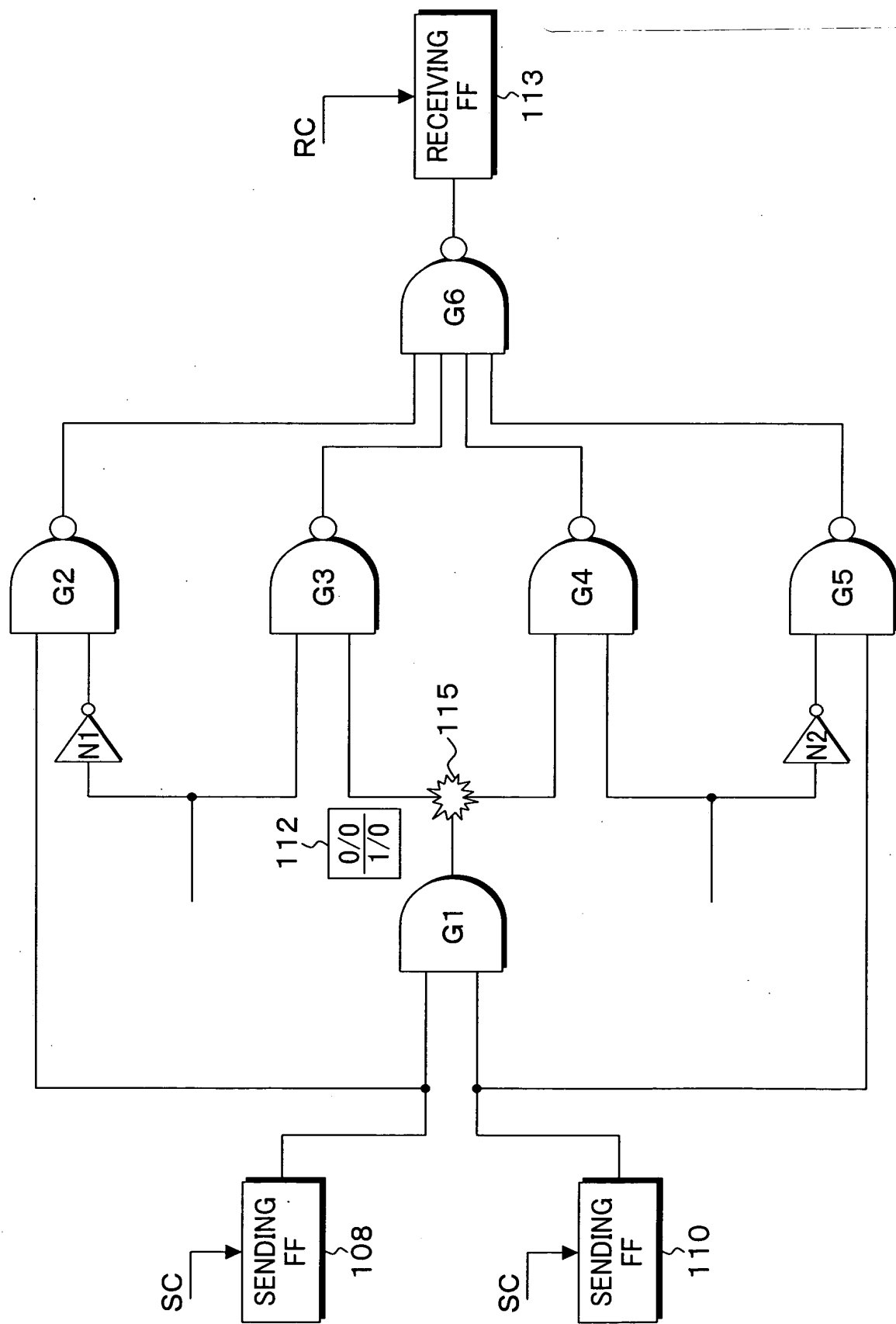
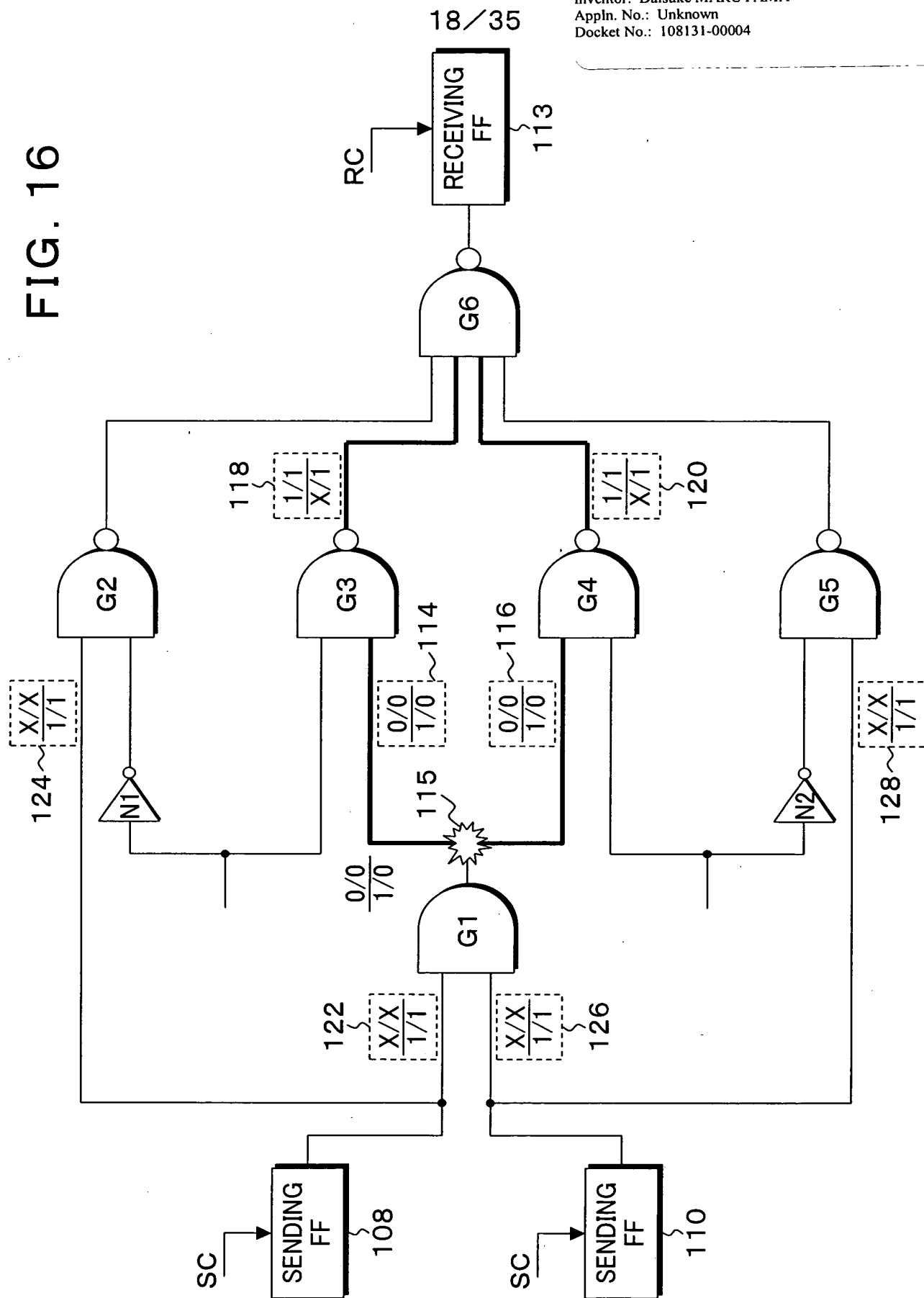


FIG. 16



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
 Inventor: Daisuke MARUYAMA
 Appl. No.: Unknown
 Docket No.: 108131-00004

FIG. 17

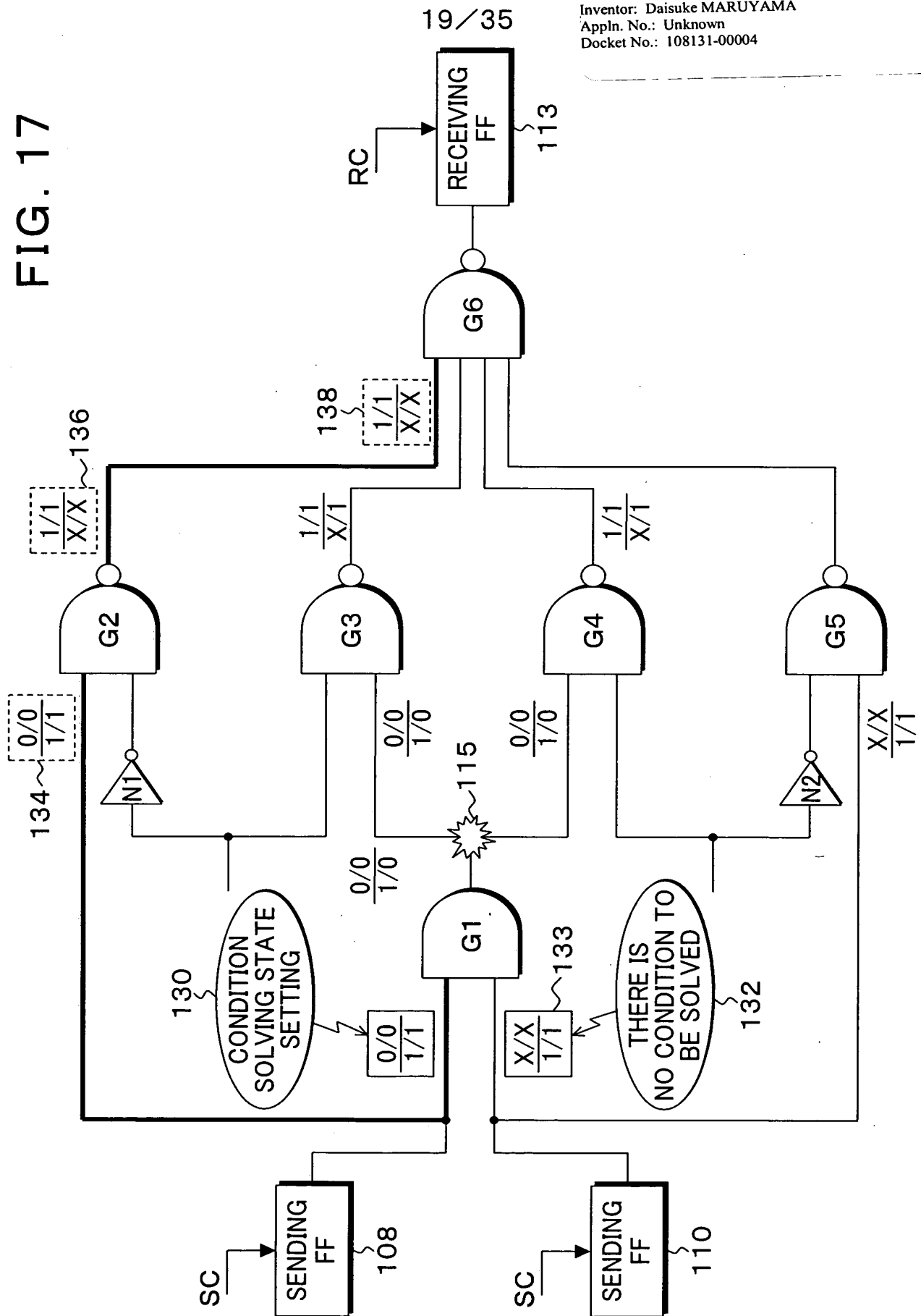


FIG. 18

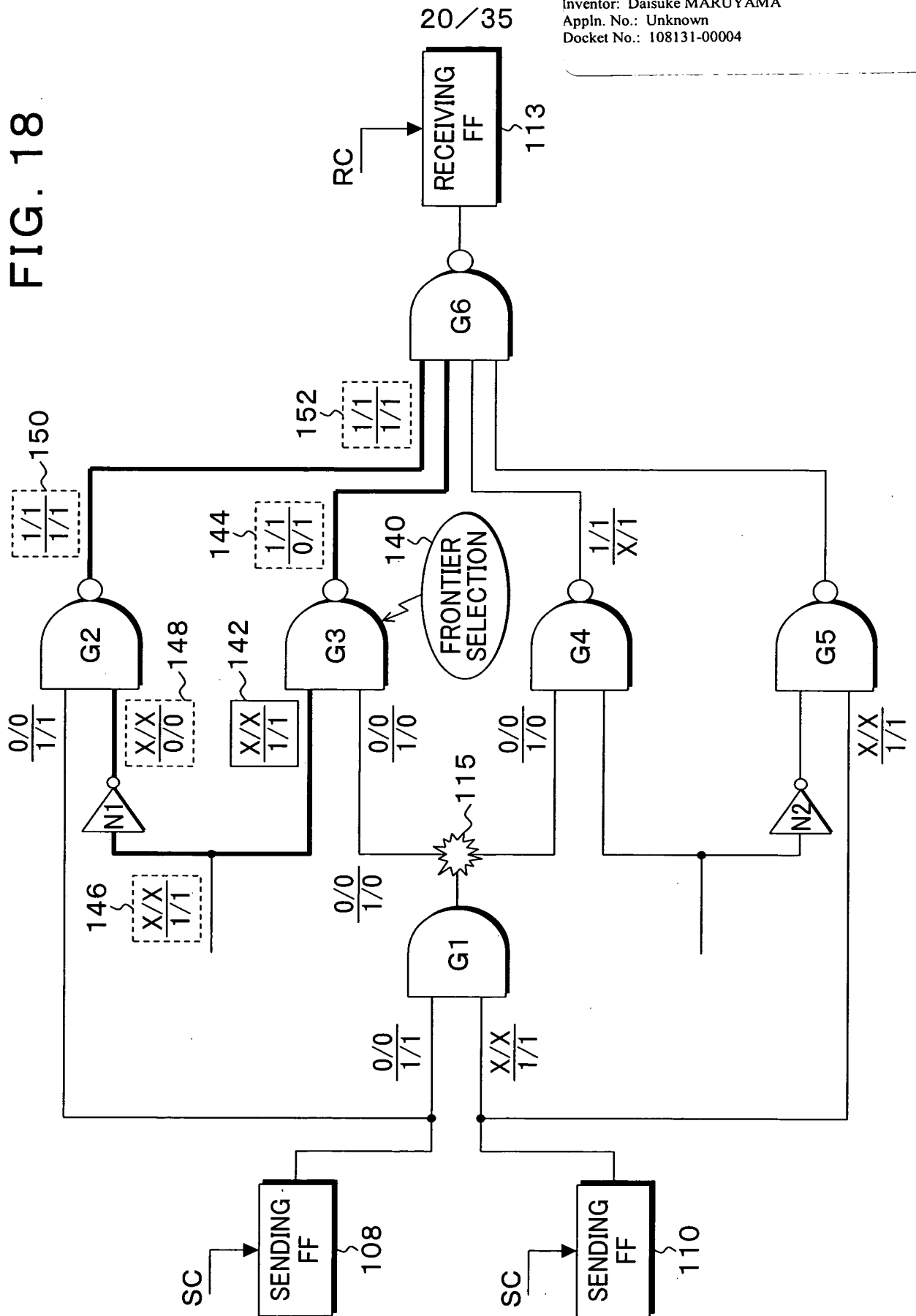


FIG. 19

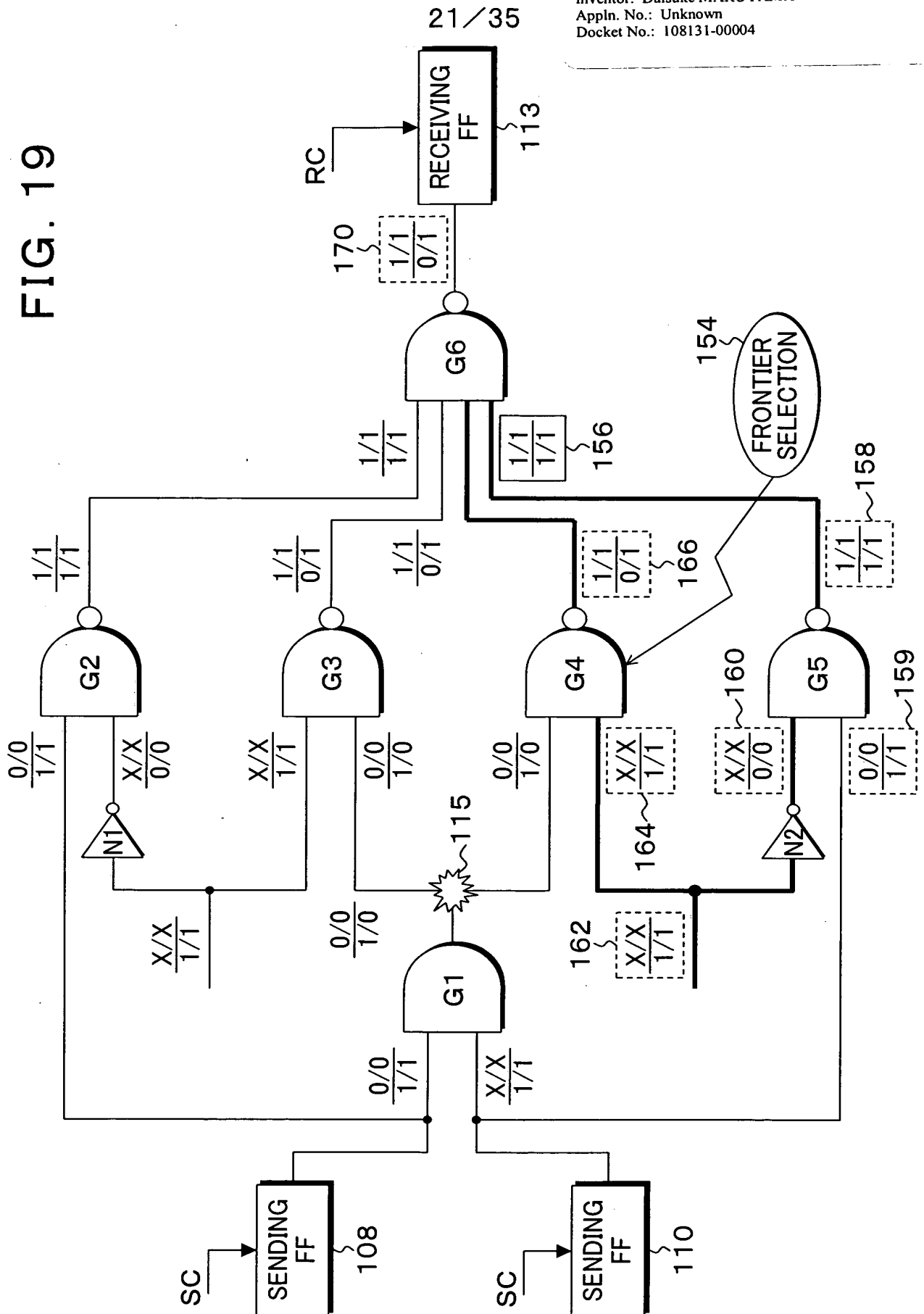


FIG. 20

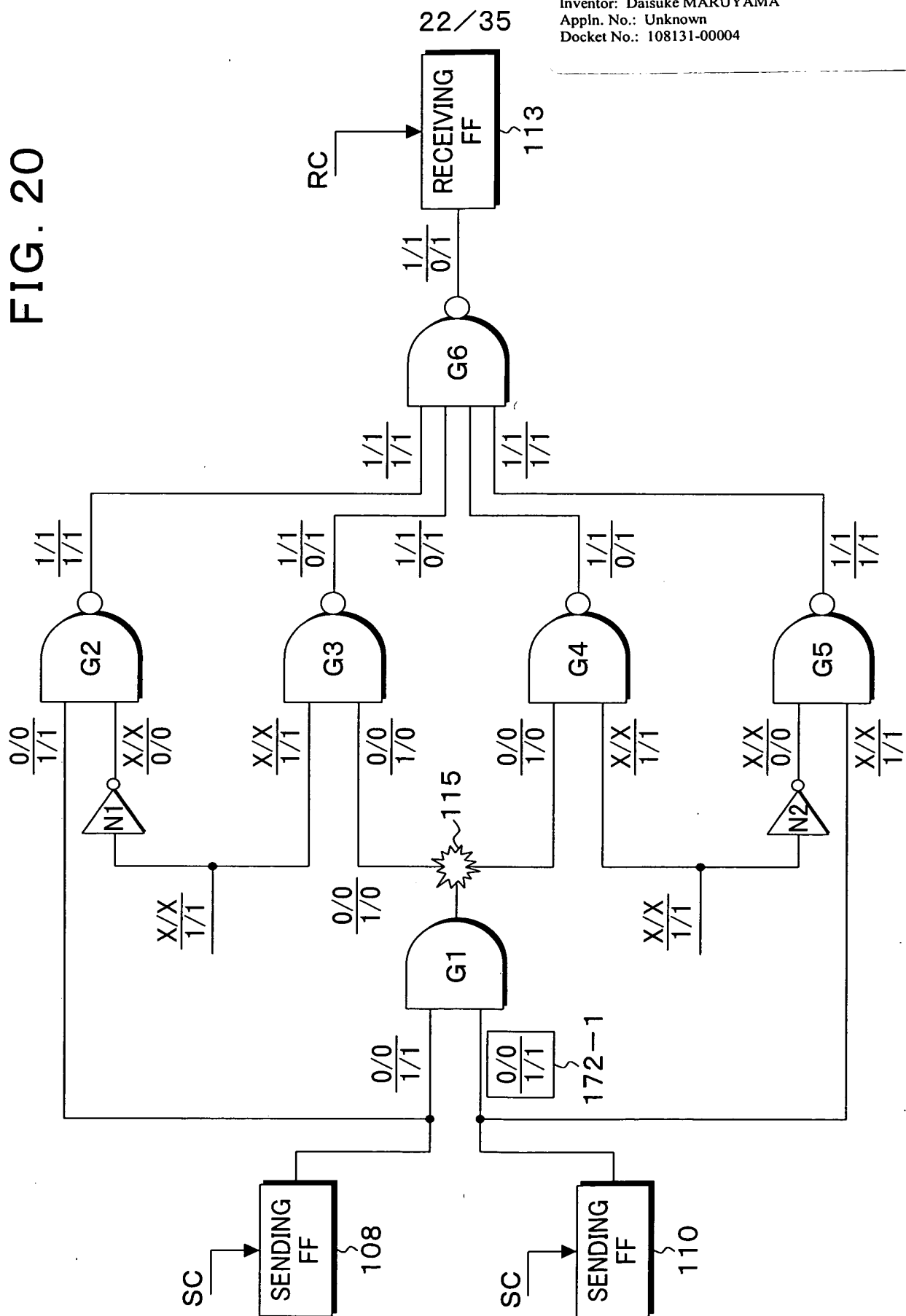


FIG. 21A

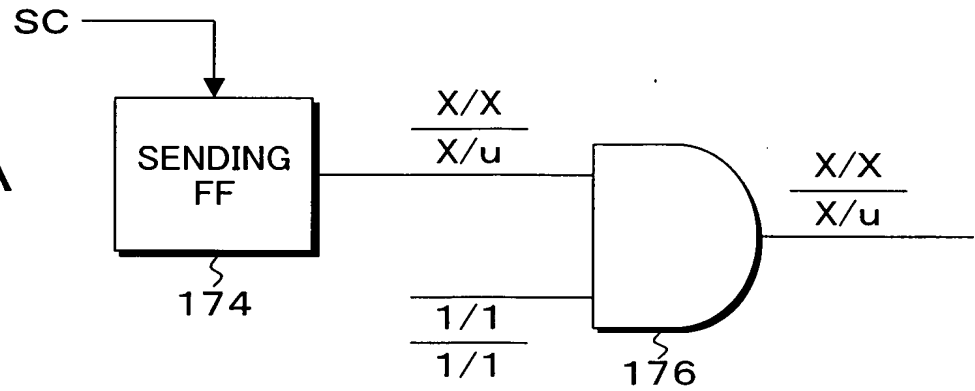


FIG. 21B

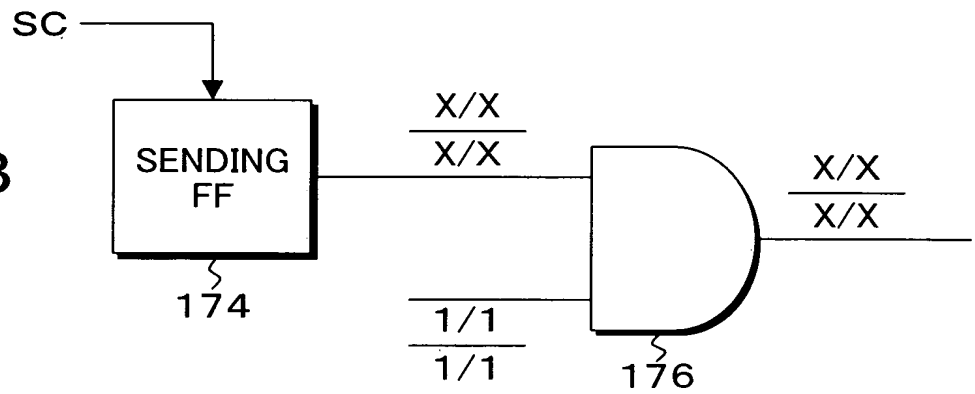


FIG. 21C

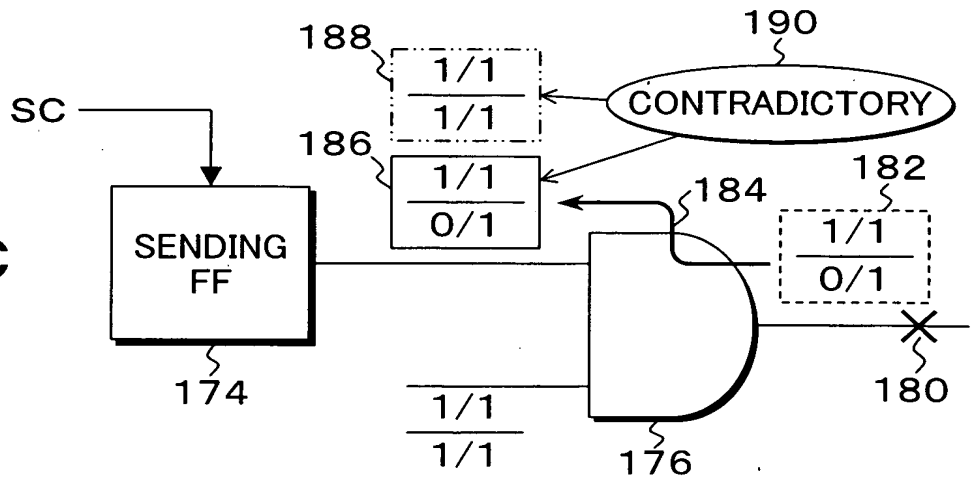


FIG. 22

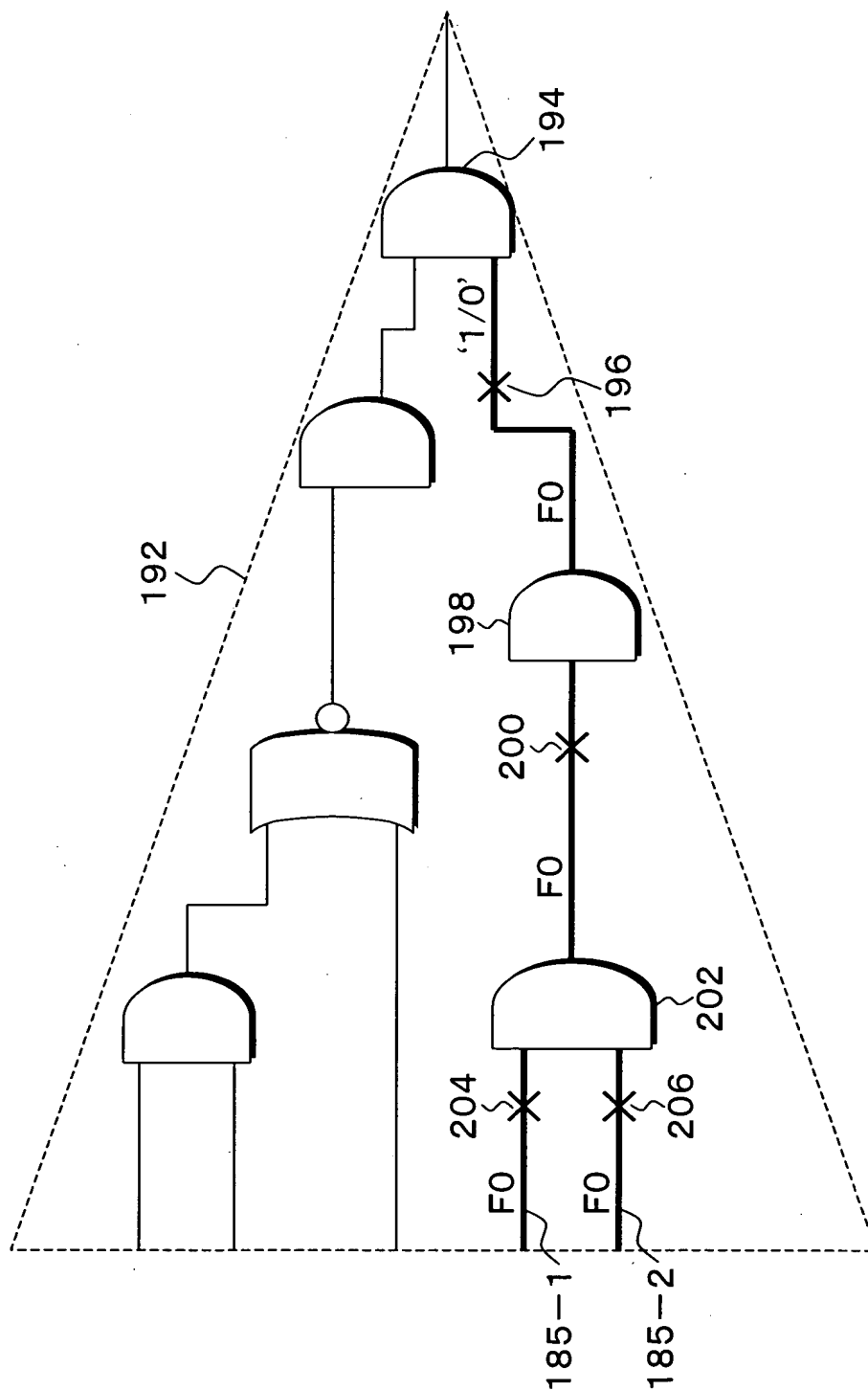


FIG. 23

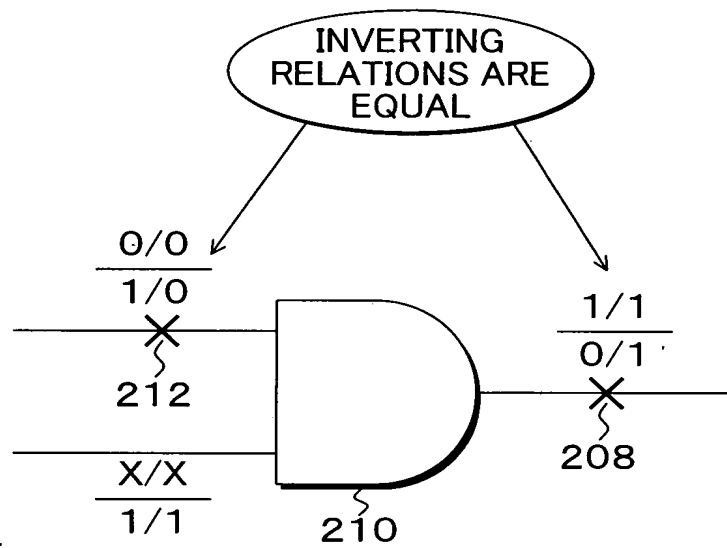


FIG. 25

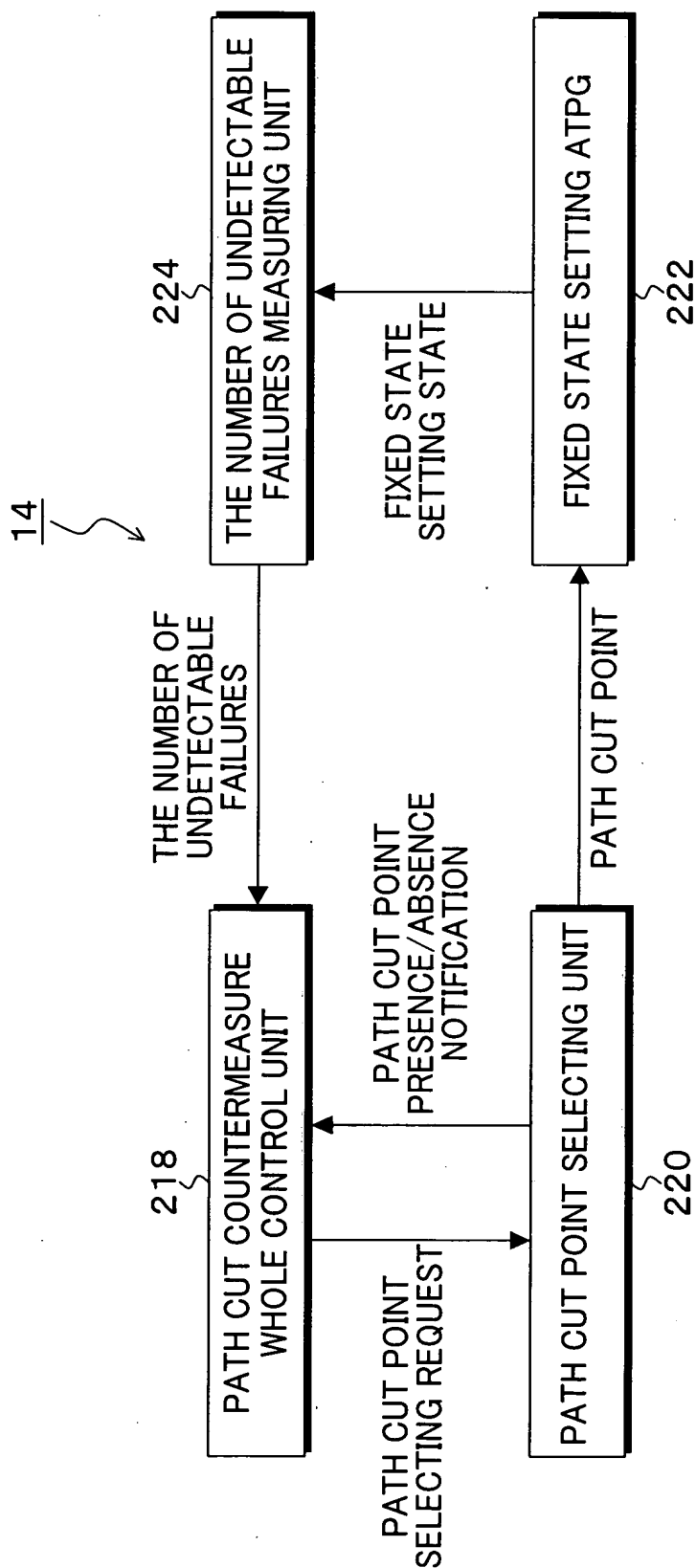


FIG. 26

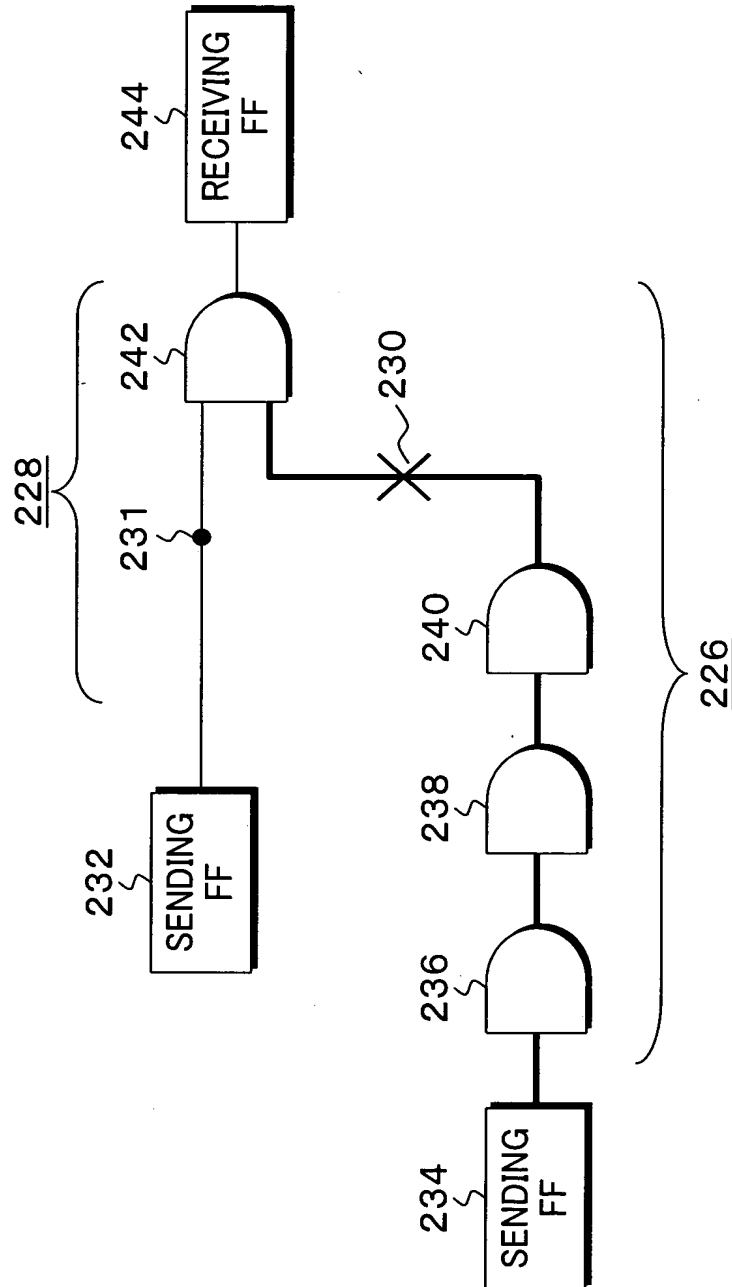


FIG. 27A

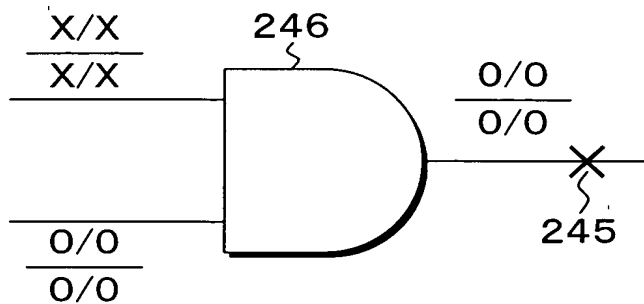


FIG. 27B

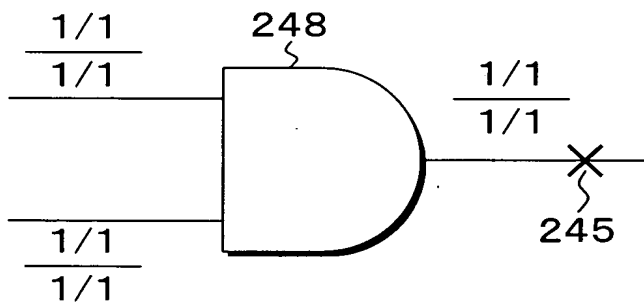


FIG. 28

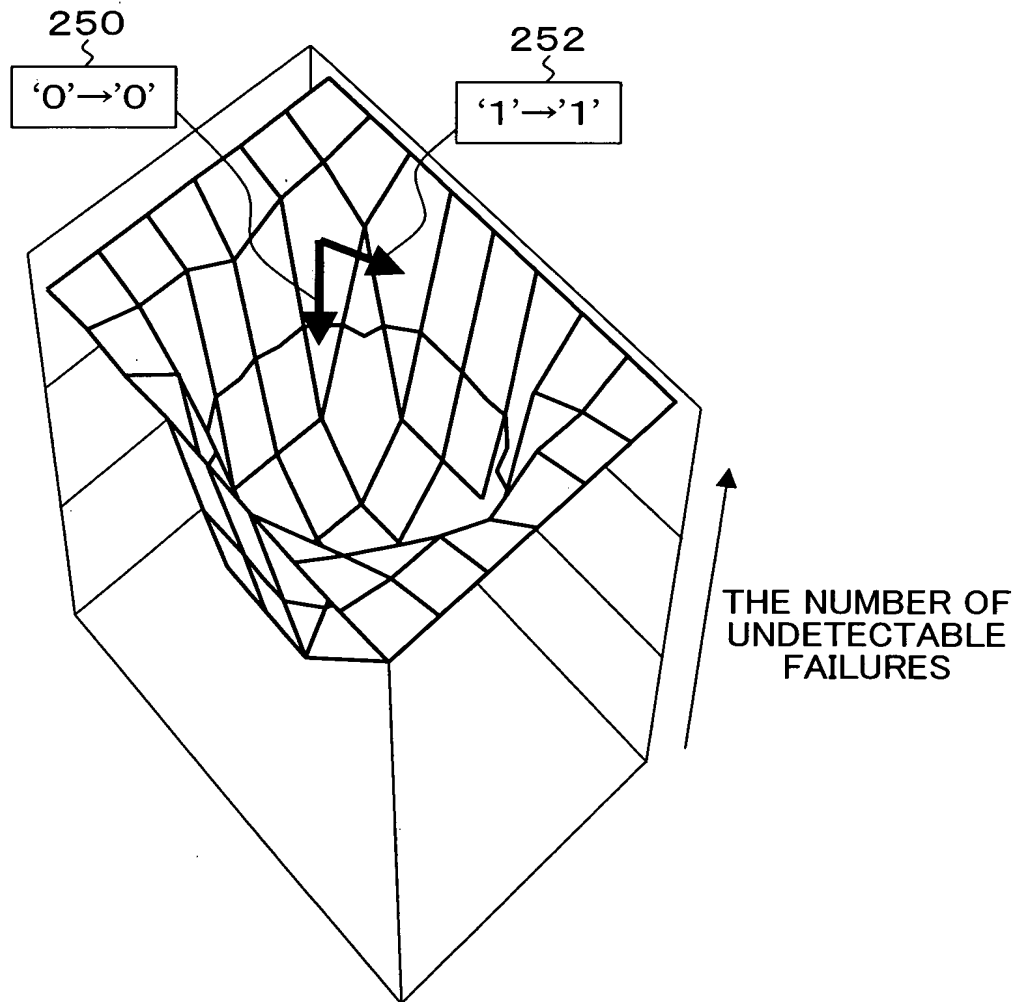
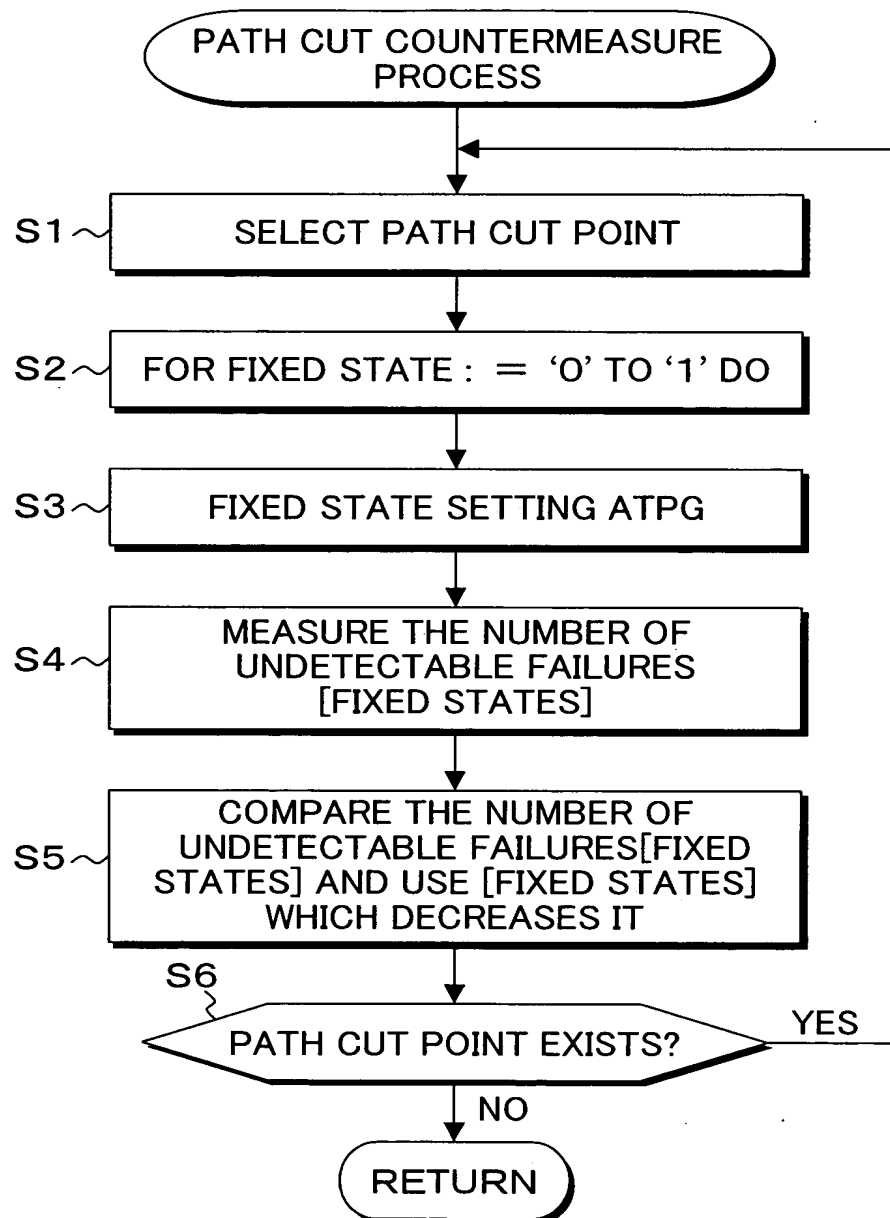


FIG. 29



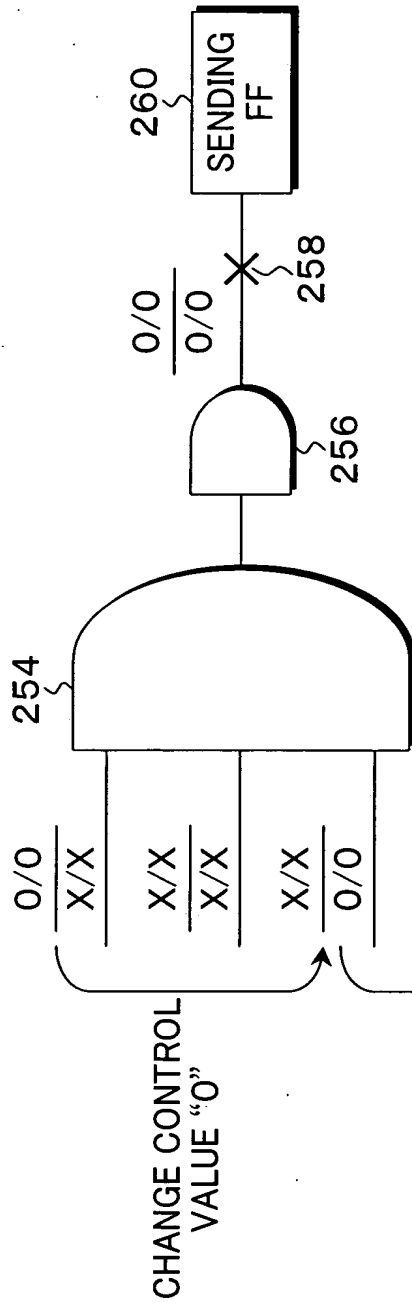


FIG. 30A

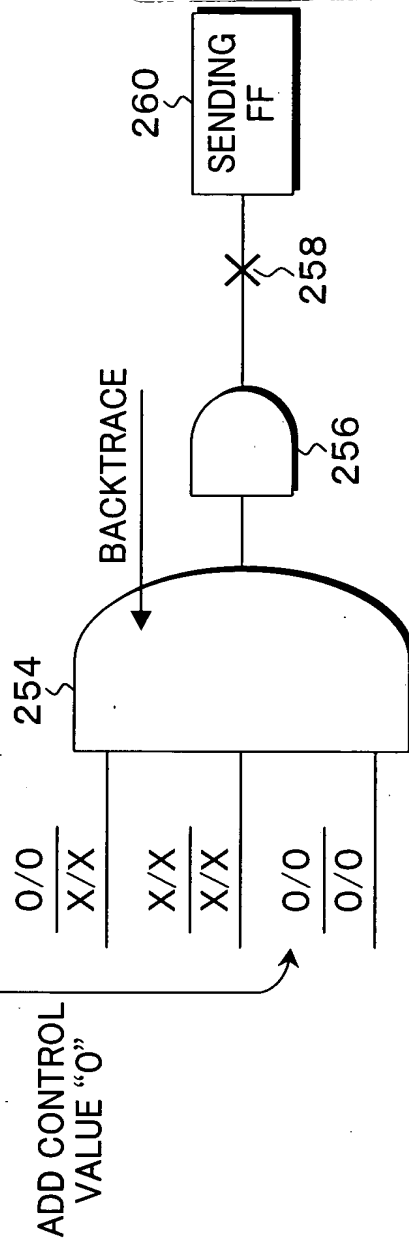


FIG. 30B

FIG. 31

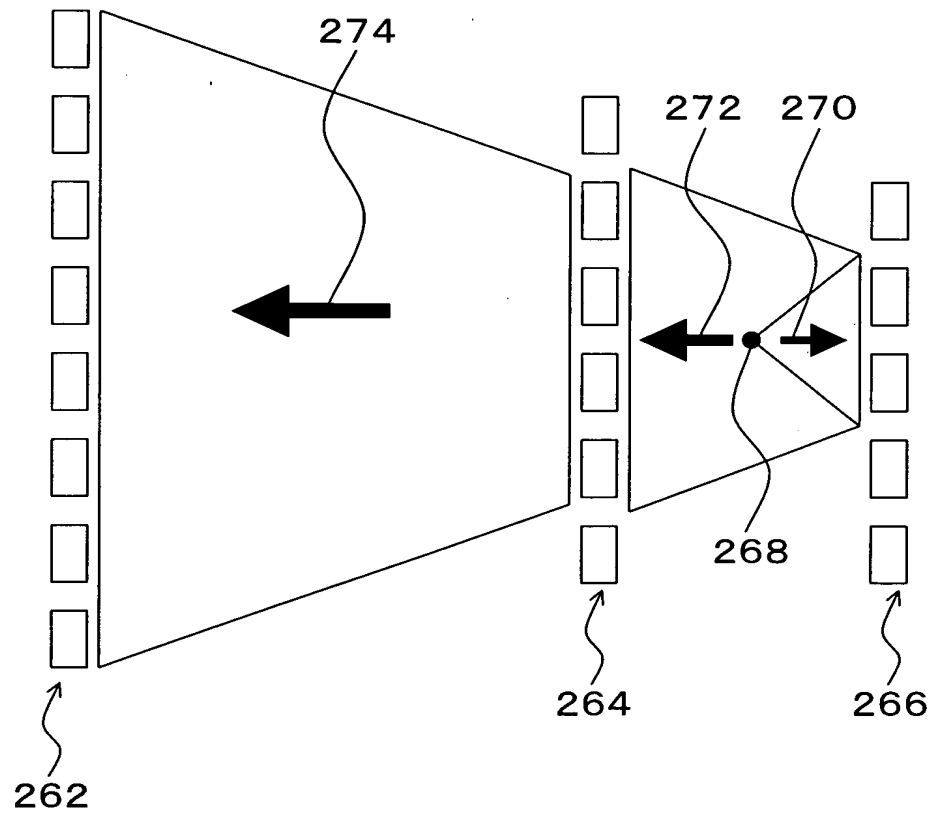


FIG. 32

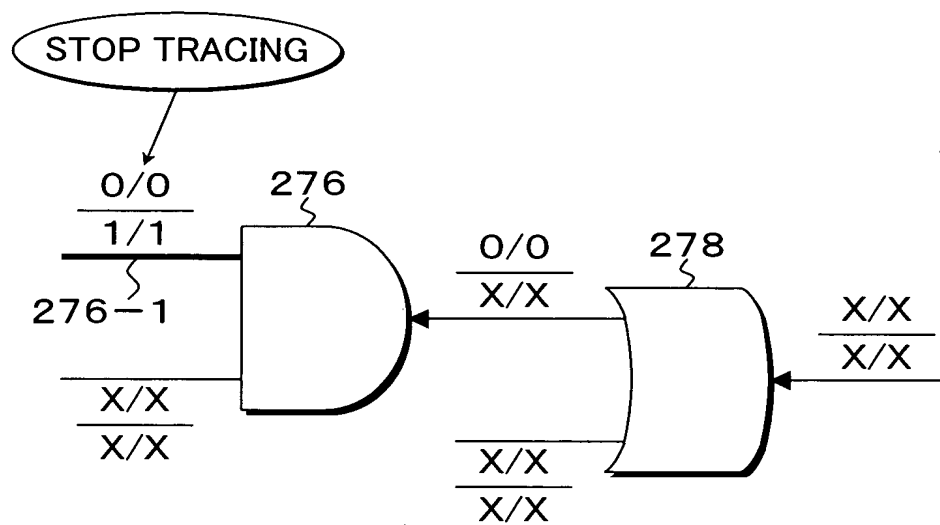


FIG. 33

